Lesson Plan

Name of the Faculty **:** Er. Vijay Kumar Anand

Discipline **:** Electronics and Communication Engineering

Semester **:** 6th

Subject **:** Digital Design using Verilog (ECE-304N)

Digital Design using Verilog Lab (ECE-312N)

Lesson Plan Duration **:** 15 weeks (from January, 2020 to April, 2020)

****Work Load (Lecture / Practical) per week (in hours) :** Lectures-03, Practical-03

Week	Theory		Practical	
	Lecture Day	**Topic (including assignment / test)**	**Practical Day**	**Experiment**
1st	1st	History of HDL, Why use HDL , Hardware design construction	1st	Basic Concepts of HDL and Digital Electronics Introduction to Model Sim , XILINX Software 1. Write a Program to implement logic gates. • AND Gate • OR Gate • XOR Gate • XNOR Gate • NOT Gate • NAND Gate • NOR Gate
	2nd	Introduction, conventional approach to digital design,		
	3rd	VLSI design, ASIC design flow		
2nd	4th	Role of HDL. Conventional Data flow, ASIC data flow	2nd	
	5th	Verilog as HDL, Levels of Design Description, Concurrency		
	6th	Simulation and Synthesis, Functional Verification, System Tasks, Programming Language Interface (PLI), Module		
3rd	7th	Simulation and Synthesis Tools, Test Benches. Language constructs and conventions	3rd	Introduction to Model Sim , XILINX Software 2. Write a Program to implement half-adder. 3. Write a Program to implement full-adder.
	8th	Keywords, Identifiers, White Space Characters, Comments,		
	9th	Numbers, Strings, Logic Values, Strengths, Data Types,		
4th	10th	Scalars and Vectors, Parameters,	4th	
	11th	Memory Operators, System Tasks.		
	12th	Assignment 1/ Class Test		
5th	13th	**Gate level modeling**: Introduction, AND Gate Primitive, Module Structure,	5th	4. Write a Program to implement 4 bit addition/subtraction. 5. Write a Program to implement a 3:8 decoder.
	14th	Illustrative Examples, Tri-State Gates,		
	15th	Additional Examples, Design of Flip-flops with Gate Primitives		
6th	16th	Delays, Strengths and Contention Resolution, Net Types, Design of Basic Circuits	6th	6.Write a Program to implement an 8:1 multiplexer.

	17th	**Behavioral modeling**: Introduction, Operations and Assignments, Functional Bifurcation,		7. Write a Program to implement a 1:8 demultiplexer
	18th	Initial Construct, Always Construct, Examples, Assignments with Delays, Wait construct,		
7th	19th	Multiple Always Blocks, Designs at Behavioral Level, Blocking and Non-block Assignments,	7th	Vive Voce- 1
	20th	Array of Instances of Primitives,		
	21st	Assignment 2/ Class test		
8th	22nd	The case statement, Simulation Flow, if and if else constructs, assign-deassign construct,	8th	8. Write a Program to implement 4 bit comparator. 9. Write a Program to implement Mod-10 up counter
	23rd	Repeat construct, for loop, the disable construct,		
	24th	**Modeling at data flow level**: Introduction, Continuous Assignment Structures,		
9th	25th	Delays and Continuous Assignments, Assignment to Vectors, Operators, Additional Examples.	9th	10. Write a program to perform serial to parallel transfer of 4 bit binary number.
	26th	Switch level modeling: Introduction, Basic Transistor Switches		
	27th	CMOS Switch, Bi-directional Gates,.		
10th	28th	Time Delays with Switch Primitives,	10th	11. Write a program to perform parallel to serial transfer of 4 bit binary number.
	29th	Instantiations with Strengths and Delays,		
	30th	Strength Contention with Trireg Nets		
11th	31st	Functions, tasks,	11th	12. Write a program to implementa8 bit ALU containing 4 arithmetic & 4 logic operations
	32nd	user defined primitives		
	33rd	Class test		
12th	34th	FSM Design (Moore and Mealy Machines),	12th	Viva voce-2
	35th	Compiler directives Parameters, Path Delays, Module Parameters,		
	36th	System Tasks and Functions, File-Based Tasks and Functions,		
13th	37th	Compiler Directives,	13th	HDL codes for the following flip-flops, SR, D, JK, T.
	38th	Hierarchical Access,.		
	39th	General Observations		
14th	40th	System tasks, functions	14th	HDL code for 4-bit binary, BCD counters (synchronous reset and asynchronous reset) and “any
	41st	While loop, forever loop,		

	42nd	Parallel blocks,		sequence" counters
15th	43rd	Force-release construct, Event	15th	Viva Voce-3
	44th	Revision		
	45th	Revision		

(Er. Vijay Kumar Anand)

Assistant Professor and Head

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