

Lesson Plan

Name of the Faculty : Er. Vijay Kumar Anand

Discipline : Electronics and Communication Engineering

Semester : 4th

Subject : Analog Circuits (EC-206A)

Lesson Plan Duration : 15 weeks (from April, 2021 to July, 2021)

****Work Load (Lecture / Practical) per week (in hours)** : Lectures-03, Practical-03

Week	Theory		Practical	
	Lecture Day	Topic (including assignment / test)	Practical Day	Experiment
1 st	1 st	Introduction to Analog Electronics, Course Objectives and Outcomes.	1 st	Design a simple common emitter (CE) amplifier Circuit using BJT and find its gain and frequency response.
	2 nd	Voltage amplifier, current amplifier, trans-conductance amplifier and trans-resistance amplifier.		
	3 rd	Biasing schemes for BJT and FET amplifiers		
2 nd	4 th	Bias stability, various configurations (such as CE/CS, CB/CG, CC/CD) and their features	2 nd	Design a BJT Emitter follower and determination of the gain, input and output impedances
	5 th	Various configurations (such as CE/CS, CB/CG, CC/CD) and their features		
	6 th	Small signal analysis of BJT Amplifier		
3 rd	7 th	Low frequency transistor models	3 rd	Design a differential amplifier using BJT and calculate its gain and frequency response
	8 th	Estimation of voltage gain, input resistance, output resistance		
	9 th	Design procedure for particular specifications		
4 th	10 th	Low frequency analysis of MSA	4 th	Viva Voce 1
	11 th	Derivation of gain, cut off frequencies		

	12 th	Assignment 1/ Class Test		
5 th	13 th	High frequency transistor models.	5 th	Design a single stage common emitter transistor amplifiers using BC107 with $V_{CC}=12V$, $V_{CEQ}=5V$, $V_E=3V$, $R_L=47K$ and $f_L=100Hz$
	14 th	Frequency response of single stage Amplifier		
	15 th	Frequency response of multistage amplifiers,		
6 th	16 th	Cascode amplifier	6 th	Design a RC coupled Single stage BJT amplifier and determination of the gain, frequency response, input and output impedances
	17 th	Class A power amplifier its power, efficiency and linearity issues		
	18 th	Class B power amplifier its power, efficiency and linearity issues		
7 th	19 th	Class AB power amplifier its power, efficiency and linearity issues	7 th	Design a self bias circuit for an NPN silicon transistor having $h_{fe}=100$ and $V_{be}=0.6V$. The desired Q-point is $V_{cc}=5V$ and $I_c=1mA$ and S or equal to 8. Assume $V_{cc}=10V$ and $R_E=1K\Omega$
	20 th	Class C power amplifier its power efficiency and linearity issues		
	21 st	Assignment 2/ Class test		
8 th	22 nd	Feedback Topologies: Voltage series, current series, voltage shunt, current shunt	8 th	Viva-Voce 2
	23 rd	Effect of feedback on gain, bandwidth calculation with practical circuits		
	24 th	Concept of stability		
9 th	25 th	Gain margin and phase margin.	9 th	Design and test the performance of BJT-RC Phase shift Oscillator for $f_0 \leq 10 KHz$
	26 th	Oscillators: Barkhausen's criterion, Sinusoidal oscillators		
	27 th	Phase shift oscillator		
10 th	28 th	Wein Bridge oscillator	10 th	Design and test the performance of BJT –Colpitt Oscillators for RF range $f_0 \geq 100KHz$.
	29 th	Resonant circuit oscillator, a general form of oscillator		
	30 th	Crystal oscillator		
11 th	31 st	LC oscillators : Hartley oscillator	11 th	Design and test the performance of BJT –Hartley Oscillators for RF range $f_0 \geq 100KHz$.
	32 nd	Colpitt oscillator		
	33 rd	Clapp oscillator		

12 th	34 th	Assignment 3/Class test	12 th	Design Schmitt trigger using op-amp and verify its operational characteristics
	35 th	Op-Amp Applications: Schmitt trigger and its applications		
	36 th	Current mirror: Basic topology and its variants, V-I characteristics,		
13 th	37 th	Output resistance and minimum sustainable voltage (VON), maximum usable load	13 th	Design an astable multivibrator using 555 timer.
	38 th	Differential amplifier: Basic structure and principle of operation		
	39 th	Calculation of differential gain		
14 th	40 th	Common mode gain, CMRR and ICMR	14 th	Design a monostable multivibrator using 555 timer
	41 st	OP-AMP design: design of differential amplifier for a given specification		
	42 nd	Design of gain stages		
15 th	43 rd	Design of output stage	15 th	Viva-Voce 3
	44 th	Revision/Quiz		
	45 th	Revision/Class test		

Er. Vijay Kumar Anand

Assistant Professor

ECE Department

ACE