

Lesson Plan

Name of the Faculty : Dr. Meenu Rani
Discipline : Electronics and Communication Engineering
Semester : 6th
Subject : Verilog HDL (EC-306A)
Lesson Plan Duration : 15 weeks (from Jan, 2026 to May 2026)

****Work Load (Lecture / Practical) per week (in hours) :** Lectures-03, Practical-03

Week	Theory		Practical	
	Lecture Day	Topic (including assignment / test)	Practical Day	Experiment
1 st	1 st	History of HDL, Why use HDL, Hardware design construction	1 st	Basic Concepts of HDL and Digital Electronics Introduction to ModelSim , Quartus Software Write a Program to implement logic gates.
	2 nd	Introduction, conventional approach to digital design,		
	3 rd	VLSI design, ASIC design flow		
2 nd	4 th	Role of HDL. Conventional Data flow, ASIC data flow	2 nd	Write a Program to implement logic gates. <ul style="list-style-type: none"> • AND Gate • OR Gate • XOR Gate • XNOR Gate • NOT Gate • NAND Gate • NOR Gate
	5 th	Verilog as HDL, Levels of Design Description, Concurrency		
	6 th	Simulation and Synthesis, Functional Verification, System Tasks, Programming Language Interface (PLI), Module		
3 rd	7 th	Simulation and Synthesis Tools, Test Benches. Language constructs and conventions	3 rd	Write a Program to implement half-adder. Write a Program to implement full-adder.
	8 th	Keywords, Identifiers, White Space Characters, Comments,		
	9 th	Numbers, Strings, Logic Values, Strengths, Data Types,		
4 th	10 th	Scalars and Vectors, Parameters,	4 th	
	11 th	Memory Operators, System Tasks.		
	12 th	Assignment 1/ Class Test		
5 th	13 th	Gate level modeling: Introduction, AND Gate Primitive, Module Structure,	5 th	Write a Program to implement 4 bit addition/subtraction. Write a Program to implement a 3:8 decoder.
	14 th	Illustrative Examples, Tri-State Gates,		
	15 th	Additional Examples, Design of Flip-flops with Gate Primitives		
6 th	16 th	Delays, Strengths and Contention Resolution, Net Types, Design of Basic Circuits	6 th	Write a Program to implement an 8:1 multiplexer. Write a Program to implement a 1:8 demultiplexer
	17 th	Behavioral modeling: Introduction, Operations and Assignments, Functional Bifurcation,		
	18 th	Initial Construct, Always Construct,		

		Examples, Assignments with Delays, Wait construct,		
7 th	19 th	Multiple Always Blocks, Designs at Behavioral Level, Blocking and Non-block Assignments,	7 th	Vive Voce- 1
	20 th	Array of Instances of Primitives,		
	21 st	Assignment 2/ Class test		
8 th	22 nd	The case statement, Simulation Flow, if and if else constructs, assign-deassign construct,	8 th	Write a Program to implement 4 bit comparator. Write a Program to implement Mod-10 up counter
	23 rd	Repeat construct, for loop, the disable construct,		
	24 th	Modeling at data flow level: Introduction, Continuous Assignment Structures,		
9 th	25 th	Delays and Continuous Assignments, Assignment to Vectors, Operators, Additional Examples.	9 th	Write a program to perform serial to parallel transfer of 4 bit binary number.
	26 th	Switch level modeling: Introduction, Basic Transistor Switches		
	27 th	CMOS Switch, Bi-directional Gates,.		
10 th	28 th	Time Delays with Switch Primitives,	10 th	Write a program to perform parallel to serial transfer of 4 bit binary number.
	29 th	Instantiations with Strengths and Delays,		
	30 th	Strength Contention with Trireg Nets		
11 th	31 st	Functions, tasks,	11 th	Write a program to implement a 8 bit ALU containing 4 arithmetic & 4 logic operations
	32 nd	user defined primitives		
	33 rd	Class test		
12 th	34 th	FSM Design (Moore and Mealy Machines),	12 th	Viva voce-2
	35 th	Compiler directives Parameters, Path Delays, Module Parameters,		
	36 th	System Tasks and Functions, File-Based Tasks and Functions,		
13 th	37 th	Compiler Directives,	13 th	HDL codes for the following flip-flops, SR, D, JK, T.
	38 th	Hierarchical Access,.		
	39 th	General Observations		
14 th	40 th	System tasks, functions	14 th	HDL code for 4-bit binary, BCD counters (synchronous reset and asynchronous reset) and “any sequence” counters
	41 st	While loop, forever loop,		
	42 nd	Parallel blocks,		
15 th	43 rd	Force-release construct, Event	15 th	Viva Voce-3
	44 th	Revision		
	45 th	Revision		

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HoD

ECE Department